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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/761,501	01/20/2004	Daniel Eddleman	LT-170	4096

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EXAMINER	
AMAYA, CARLOS DAVID	
ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 06/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/761,501	EDDLEMAN, DANIEL	
	Examiner	Art Unit	
	Carlos Amaya	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01/20/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-11* is/are allowed.

6)☐ Claim(s) *12-14,16-20* is/are rejected.

7)☐ Claim(s) *15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 July 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/18/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 1A-1B and 2A-2D should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities: On page 7 applicant fails to provide the number of a co-pending US Patent Application directed to current mirrors. Also on page 6 line 18 Applicant refers to a "reference voltage V_F", but on Figure 3 the reference voltage is V_E. Appropriate correction is required.

Claim Objections

3. Claim 12 is directed to a method, but on page 26 line 8 Applicant recites the phrase "the circuit comprising", when it should read "the method comprising". Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 12-14, 16-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Nercessian (US 3,623,140).

With respect to claim 12 Nercessian discloses a method for controlling an output of a slave supply (Slave supply 1) in a defined relationship to a time- varying master signal (Figure 2 shows a master and slave programmable power supplies, the master signal varies in time with respect to variable resistor 28, 14 and Programming voltage source 15), the slave supply having a slave output terminal (Slave output terminal 4) and a feedback input terminal (Slave supply inverting input 2), the method comprising: varying the master signal at a master ramp rate (The master signal is varied by varying the resistance of resistor 14, 28 and Programming voltage source 15 Figure 2); generating current responsive to the master signal (Column 2 lines 66-72); injecting the generated current into the feedback input terminal of the slave supply (The generated current by master supply 8 is injected to the feedback terminal 2 of the slave supply, which receives this feedback signal from the junction of resistors 23 and 25); forcing the output of the slave supply to vary responsive to the master signal and in accordance with the defined relationship (Column 2 lines 66-69); and presenting a high impedance to the feedback input terminal of the slave supply (the impedance of the feedback input

terminal of the slave supply is determined by the master supply 8, which depends on the varying master signal, thus to have high impedance the resistors 14, 28 and the programming voltage source 15 have to be taken into account).

With respect to claim 13 Nercessian discloses the method of claim 12, further comprising changing the ramp rate of the master signal with respect to time (The ramp rate signal and thus the output of the master supply 8 is change with respect to resistors 14, 28 and voltage source 15, thus by changing the one of the parameters the signal is change with respect to time).

With respect to claim 14 Nercessian discloses the method of claim 12, wherein forcing the output of the slave supply to vary comprises forcing the output of the slave supply to ramp at the same rate as the master ramp rate (By changing the master signal this signal in turns changes the output of the slave supply at the same rate, Column 2 lines 66-69).

With respect to claim 16 Nercessian discloses the method of claim 12, further comprising user-programming the defined relationship (Figure 2 shows a master and slave programmable power supplies, the user programs/changes the resistors 14, 28 and voltage source 15).

With respect to claim 17 Nercessian discloses the method of claim 16, wherein user- programming the defined relationship comprises selecting at least one resistance value (Either of resistor 14 or 28 can be selected /change by a user).

With respect to claim 18 Nercessian discloses the method claim 12, further comprising of generating the master signal. The master signal is generated with respect to resistors 14, 28 and programming voltage source 15.

With respect claim 19 Nercessian discloses the method of claim 18, wherein generating the master signal comprises generating the master signal from a master power supply (Master power supply 8 generates the master signal with resistors 14, 28 and programming voltage source 15).

With respect to claim 20 Nercessian discloses a method for controlling an output of a power supply in a defined manner, the method comprising: providing a power supply (Master power supply 8) with a feedback terminal (Feedback terminal consisting of variable resistor 28 connected to leads 29 and 30 and load terminal 21), an output terminal (Load terminal 21) and a feedback network coupled between the feedback terminal and the output terminal (Feedback terminal and the output terminal are couple together as shown in Figure 2), the feedback network presenting a resistance (resistor 28) between the output terminal and the feedback terminal; dynamically changing the resistance of the feedback network (Resistor 28 is a variable resistor, a user changes its resistance); and modifying the output of the power supply responsive to the dynamically changing resistance of the feedback network (Depending upon the resistance 28 the master supply is changed, Column 3 lines 4-8).

Allowable Subject Matter

6. Claims 1-11 are allowed over the prior art of record, because the prior art of record does not disclose or suggest "a charging circuit for supplying a drive signal to a ramp generator circuit configured to generate the master signal, the charging circuit having first and second current sources for selectably sourcing current to or sinking current from the ramp generator circuit; a tracking input terminal for receiving a tracking signal responsive to the master signal" and "a third current source coupled to the circuit output terminal that generates output current responsive to the op amp output signal, the output current having a magnitude that forces the output of the slave supply to behave in the defined relationship to the master signal when the circuit output terminal is coupled the feedback input terminal, and the coupling of the third current source to the circuit output terminal presenting a high impedance to the feedback input terminal". Along with the remaining features of the claim.

7. Claim 15 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. Claim 15 is allowable over the prior art of record, because the prior art of record does not disclose, "adding a time delay between onset of ramping the master signal and onset of ramping the output of the slave supply".

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to the examiner's supervisor, Brian Sircus who can be reached on (571)272-2800. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CA

CHAU N. NGUYEN
PRIMARY EXAMINER